REMARKS

I. Introduction

Claims 1-7 are pending in this application. In this Amendment, claims 1-7 have been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the written description of the specification.

II. The Rejection of Claims 1 under 35 U.S.C. §112, Second Paragraph

Claim 1 has been rejected under 35 U.S.C. §112, second paragraph, because the meaning of the phrase "if the same description block is performed at the same time" is purportedly unclear.

In response, the phrase has been amended as follows: "every time the first row in the description block is executed during that simulation time." Applicant believes this amendment is fully responsive to the Examiner's concern regarding claim 1. Withdrawal of the rejection of claim 1 under 35 U.S.C. §112, second paragraph is, therefore, respectfully solicited.

III. The Rejection of Claims 1-7 under 35 U.S.C. §101

Claims 1-7 have been rejected under 35 U.S.C. §101 because the claimed invention is purportedly directed to non-statutory subject matter. The Examiner asserted as follows: "[a]s per claim 1, deleting a previous history of the description block does not result in a tangible product," and "[a]s per claims 2-7, analyzing the executed rows fails to product a tangible result."

In response, Applicant has amended claims 1-7, respectively, to recite additional limitations related to the limitations identified by the Examiner. Applicant believes that the claimed invention is now directed to statutory subject matter, and respectfully solicits withdrawal of the rejection of the claims under 35 U.S.C. §101.

IV. The Rejection of Claim 1 under 35 U.S.C. §102(e)

Claim 1 has been rejected under 35 U.S.C. §102(e) as being anticipated by Hekmatpour. In the statement of the rejection, the Examiner asserted that Hekmatpour discloses a method for verifying the design of a microprocessor identically corresponding to what is claimed. This rejection is respectfully traversed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Applicant submits that Hekmatpour does not disclose a simulation method including all the limitations recited in claim 1. Specifically, the reference does not disclose, at minimum, "generating an executed-row history for the description block indicating an executed description row in the simulation time," and "every time the first row in the description block is executed during that simulation time, deleting the executed-row history previously generated in the simulation time and generating a new executed-row history for the description block," recited in claim 1.

The Examiner asserted that Hekmatpour in column 10, lines 18-44 discloses the above-cited limitations of claim 1. The Examiner's cited portion describes that "coverage estimator 212 is adapted to analyze generic test description 210 with respect to the test specification indicated by verification engineer and optimized by test specification optimizer 204 and to determine what, if any, new states or transitions are potentially exercised by the test description 210" (column 10, lines 39-44). In other words, this portion simply describes performing analysis of generic test description 210. It is apparent that Hekmatpour is silent on generation of an executed-row history for a description block, deletion of the executed-row history previously generated in the simulation time, and generation of a new executed-row history for the description block, as recited in claim 1.

The above-described fundamental differences between the claimed invention and Hekmatpour make it clear that Hekmatpour does not identically describe the claimed invention within the meaning of 35 U.S.C. §102. Applicant, therefore, submits that the imposed rejection of claim 1 under 35 U.S.C. §102(e) for lack of novelty as evidenced by Hekmatpour is not factually viable and, hence, respectfully solicits withdrawal thereof.

V. The Rejection of Claims 2-7 under 35 U.S.C. §102(b)

Claims 2-7 have been rejected under 35 U.S.C. §102(b) as being anticipated by McNamara et al. In the statement of the rejection, the Examiner asserted that McNamara et al. discloses a system for automated design verification identically corresponding to what is claimed.

Applicant first notes that the rejection of claims 2-4 and 7 has been rendered moot by the amendment of changing these claims to be dependent on independent claim 1.

Applicant also submits that McNamara et al. does not disclose an emulation method including all the limitations recited in claim 5. Specifically, the reference does not disclose, at minimum, "analyzing correspondence information that represents correspondence between combinations of the signals used in hardware emulation process which correspond to input signals to the description block and executed rows," recited in claim 5.

The Examiner asserted that McNamara et al. in column 4, lines 28-36 discloses the above cited limitation of claim 5. The Examiner's cited portion describes as follows (emphasis added):

> The test generator 106 automatically constructs a first set of test vectors for causing each state of the state machine to be visited and each transition arc to be taken. This first set of test vectors proves whether each of the basic blocks that make up the design description is correct. The test generator 106 then produces a second set of test vectors for proving that user-selected subsets of the basic blocks work together correctly. These subsets of the basic blocks, when linked together, are equivalent to the paths of interest discussed above.

McNamara describes constructing vectors for proving whether basic blocks are correct and whether user-selected subsets of the basic blocks work together correctly. In contrast, claim 5 recites "analyzing correspondence information that represents correspondence between combinations of the signals used in hardware emulation process which correspond to input signals to the description block and executed rows." Applicant stresses that analyzing the correspondence information representing the correspondence between the signals and the executed rows in the claim is different from constructing vectors proving whether blocks are correct, and the Examiner did not provide any reason why the claimed information and McNamara's vectors are the same. This argument is applicable to claim 6 reciting "analyzing executed rows based on the correspondence information that represents the correspondence between the input conditions and the executed rows and a tracing result of the input signal to the description block."

Based on the foregoing, Applicant submits that McNamara et al. does not disclose all the limitations recited in claims 2-7 within the meaning of 35 U.S.C. §102(b). Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1-7 under 35 U.S.C. §102(b), and favorable consideration thereof.

VI. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:TT
Facsimile: 202.756.8087
Date: July 10, 2006